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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,436	06/23/2003	Jong-Jan Lee	SLA 0733	9661

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,436	LEE ET AL.	
	Examin r	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06232003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction/Elections

1. Applicant's election without traverse of Claims 12 – 30 in Letter of March 24, 2004 is acknowledged.

Claim Rejections – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 12, 13, 16 – 19, 22, 23, 25, and 27 - 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (US 6,475,869 B1).

4. Regarding Claim 12, Yu discloses a method of fabricating a strained silicon finFET device, comprising the steps of:

providing a silicon on insulator (SOI) substrate having a silicon containing multilayer (16) (Figure 3) on an insulator layer (18) (Col. 4, lines 7 – 8),

patterning the multilayer into a source region (22) and a drain region (24) (Figure 1) (Col. 4, line 3) sandwiching a seed channel region (16), the seed channel being a seed fin structure (Col. 4, lines 14 – 19),

depositing an epitaxial channel layer onto the seed fin structure (38) (Figure 7) (Col. 5, lines 54 – 57), the channel layer material (SiGe) having a lattice constant different that that of the seed fin material (silicon) wherein the epitaxial channel layer becomes a strained channel layer (Col. 2, lines 26 – 27) due to lattice mismatch between channel layer and seed fin structure,

forming a gate dielectric layer (34) Figure 8) (Col. 4, lines 39 – 44) on the epitaxial strained channel, and

forming a gate (36) (Figures 1, 2) over the epitaxial strained channel.

5. Regarding Claim 13, Yu discloses that the silicon containing multilayer comprises silicon (Col. 4, lines 7 – 10).

6. Regarding Claim 16, Yu discloses that the epitaxial channel layer is a silicon germanium layer (Col. 5, lines 54 – 57).

7.Regarding Claim 17, Yu discloses that conventional lithographic processes (Col. 5, lines 26 – 28) (Col. 6, lines 30 – 32) are used in patterning and defining channel and adjacent source/drain regions, whereinafter, the mask is removed to yield the structure shown in Figure 1.

8. Regarding Claim 18, Yu discloses (Col. 2, lines 31 – 34) that the channel region is doped within the epitaxial chamber. (Col. 2, lines 31 – 34)

9. Regarding Claim 19, Yu discloses that formation of the gate comprises the steps of:

depositing a gate material layer (36) (Figure 2),

doping the gate material layer (Col. 4, lines 45 – 47),

patterning and defining the gate (36) using conventional lithographic processes (Col. 6, lines 28 – 32) and subsequently removing mask.

10. Regarding Claim 22, Yu discloses that the multilayer comprises:

a first silicon-containing layer (16) (Figure 3), and

a second silicon-containing layer (SiGe) having a lattice constant different that that of the first material (silicon) wherein the second layer (38) becomes a strained layer (Col. 2, lines 26 – 27) due to lattice mismatch between channel layer and the first layer.

11. Regarding Claim 23, Yu discloses that the multilayer is formed by providing a silicon on insulator substrate (14) having a first silicon containing layer (16) (Figure 3), and depositing a second silicon-containing layer (38) on the silicon on insulator substrate, wherein the lattice constant of the second material is different from that of the first layer, resulting in a strained layer (Col. 2, lines 26 – 27).

13. Regarding Claim 25, Yu discloses that the first silicon containing layer (16) is a silicon layer (Col. 4, lines 8 – 10) and the second silicon containing layer (38) is a silicon germanium layer (Col. 5, lines 55 – 58).

14. Regarding Claim 27, Yu discloses that the top most layer of the multilayer (40) comprises a hard mask layer (Col. 5, lines 23 – 25).

15. Regarding Claim 28, Yu discloses that the height of the fin structure(32) (Figure 8) is 50 – 80 nm, well within the range recited in the instant application. (Col. 4, lines 17 – 18).

16. Regarding Claim 29, Yu discloses that the width of the fin structure(32) (Figure 8) is 10 – 30 nm, well within the range recited in the instant application. (Col. 4, lines 17 – 18).

17. Regarding Claim 30, Yu discloses that the thickness of the strained channel layer is 5 to 10 nm, well within the range recited in the instant application. (Col.5, lines 57 – 58).

Claim Rejections – 35 U.S.C. 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to Claims 12, 13, 16 – 19, 22, 23, 25, and 27 – 30, and further in view of Cheng et al. (US 6,737,670 B2).

20. Regarding Claim 14, Yu does not disclose the presence of an SGOI substrate wherein the silicon containing multilayer comprises a SiGe layer. Cheng et al. disclose an SGOI substrate (Figure 1B) with a SiGe layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the growth procedures of Cheng et al. in Yu to provide a relaxed SiGe layer for fabrication of a SiGe fin structure to further improve electron mobility.

21. Regarding Claim 15, Yu do not disclose the composition of an SiGe layer used in the SGOI substrate. Cheng et al. disclose (Col. 3, lines 31 – 40) that the germanium content is less than 25% within the layer, so that the seed fin fabricated from the layer is also <25%, in agreement with the recited range of the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the growth procedures of Cheng et al. in Yu to provide a SiGe layer to further improve electron mobility.

22. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to Claims 12, 13, 16 – 19, 22, 23, 25,and 27 – 30, and further in view of Assaderaghi et al. (US 6,432,754 B1).

23. Regarding Claim 20, Yu discloses that source and drain extensions are formed adjacent to channel region (Col. 4, lines 29 – 30). Yu does not disclose the formation of "halo" regions between the channel and source/drain regions. Assaderaghi et al. disclose (Col. 5, lines 15 – 27) the formation of "halo" implant regions (32) (Figure 4) between channel and source/

drain regions in a device formed on an SOI substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Assaderaghi et al. with Yu to produce halo implant regions adjacent to the channel region that provide adjustment of punchthrough voltage and threshold voltage.

24. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to Claims 12, 13, 16 – 19, 22, 23, 25,and 27 – 30, and further in view of Gambino et al. (US 6,689,650 B2) and Literature Digest ("The Highlights of the IEDM 2002," vol. 6, (March, 2003) pp. 1 – 6)

Yu discloses a method, comprising:

doping source/drain regions (22,24) (Col. 4, lines 31 – 38), and

forming silicides on source/drain regions (Col. 5, lines 7 – 9).

Yu does not disclose forming dielectric spacers between gate and source/drain regions. In a FinFET structure, Gambino et al. disclose the formation of spacers (36) (Figures 11A,11B) between gate (40) and source/drain regions (42). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Gambino et al. with Yu to obtain damage protection layers at the edge of the gate.

Additionally, Yu does not disclose the formation of a silicide on the gate region. However, the implementation of silicided gates on finFET structures is disclosed in Literature Digest (page 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Literature Digest with Yu to obtain a silicided gate to reduce poly depletion effects.

25. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, as applied to Claims 12, 13, 16 – 19, 22, 23, 25, and 27 – 30, and further in view of Bae et al. (US 6,633,066 B1).

26. Regarding Claim 24, Yu does not disclose the thickness of the first silicon containing region. Bae et al. disclose for an SOI structure containing a silicon first layer and a SiGe second layer (Figure 3E) that the thickness of the first layer (18) is 200 Angstroms (20 nm). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Bae et al. with Yu to obtain a silicon thickness that will result in strain within the overlying second layer to produce mobility enhancement.

27. Regarding Claim 26, Yu does not disclose the germanium concentration in the SiGe layer. Bae et al. disclose (Col. 7, line 45) that the Ge concentration is 40 percent for the Si(I-x)Ge(x) layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Bae et al. with Yu to obtain a SiGe layer that would produce mobility enhancement.

Conclusions

28. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the

examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

ORI NADAV
patent examiner

Thomas Magee
May 30, 2004